HTG9696A-31B-28C05

产品名称（**Product name**） ：黑白点阵 COG

型　　号（**Model**） ：HTG9696A-31B-28C05

编　　号（**Part number**） ：20140809

日　　期（**Date**） ：2014-08-18

深圳市鑫洪泰电子科技有限公司 **Shenzhen Hot Display Technology Co.,Ltd**		
编制 **Prepared by**	审核 **Checked by**	核准 **Approved by**

编码：QR-R-011　A/0　　序号：

Rev.	Descriptions	Date
01	Prelimiay Release	2014-08-18

Table of Content

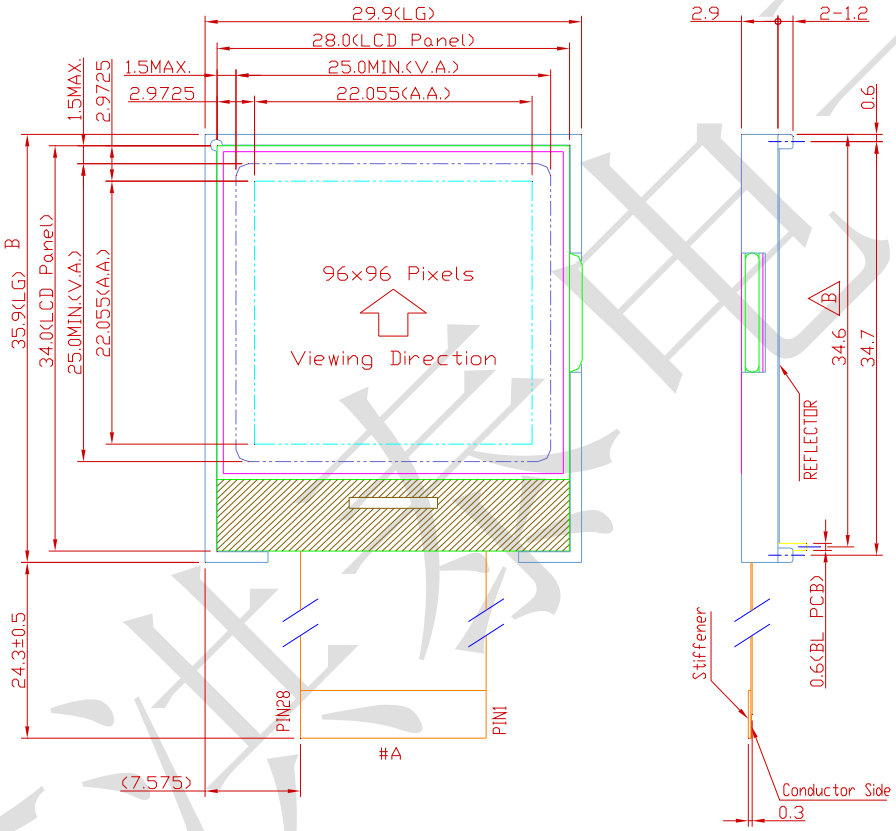
1. Bsaic Specifications

1.1 Display Specifications

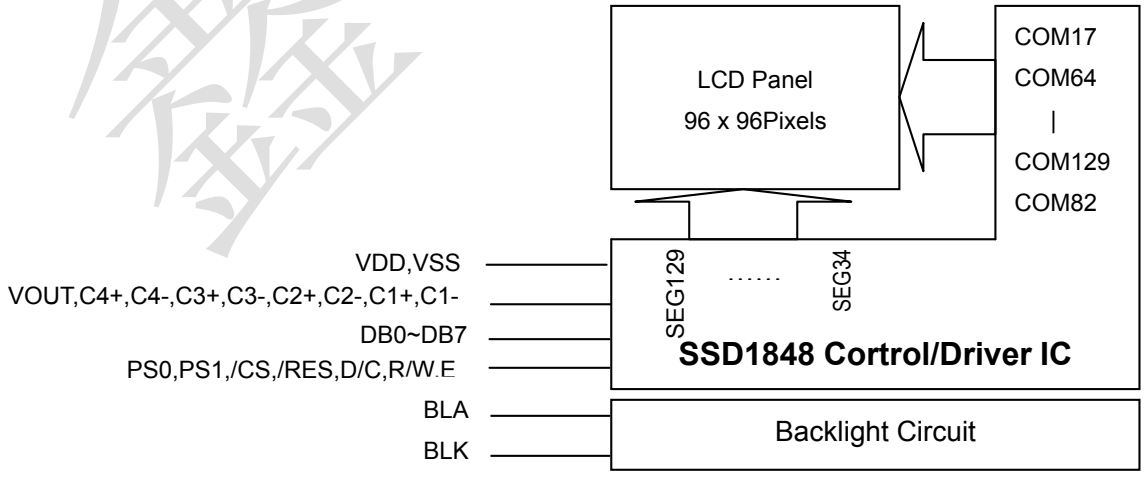
1>LCD Display Mode : FSTN, Positive, Transflective
2>Viewing Angle : 6H
3>Driving Method : 1/96 Duty, 1/11 Bias
4>Backlight : Blue LED

1.2 Mechanical Specifications

1>Outline Dimension : 29.9x 35.9 x 2.8mm (See attached Outline Drawing for Details)



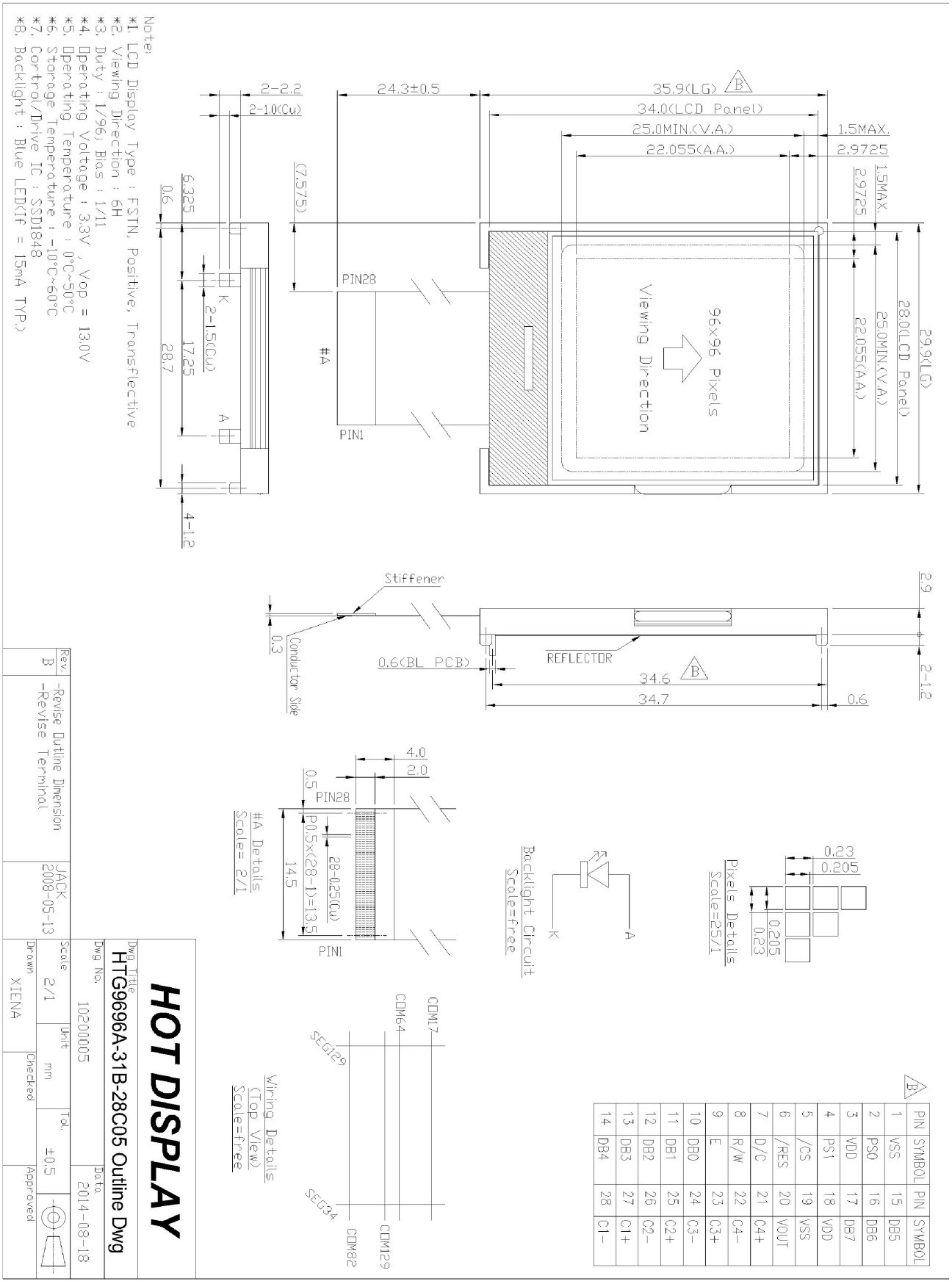
1.3 Circuit Diagram



1.4 Terminal Function

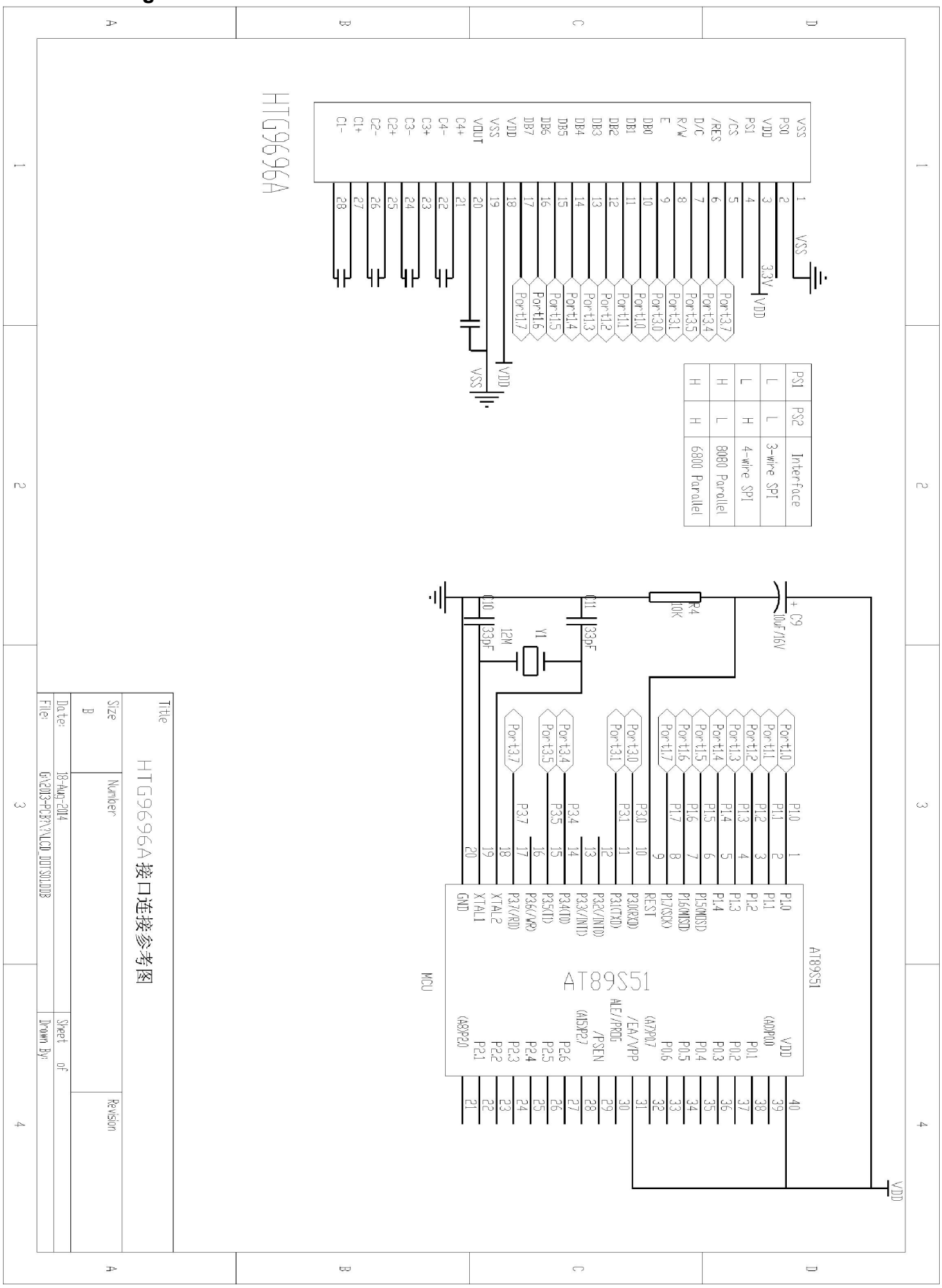
<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>Function</th></tr>
<tr><td>1</td><td>VSS</td><td>This is a logic ground pin. It must connect to GND from external supply</td></tr>
<tr><td>2</td><td>PS0</td><td>PS0 and PS1 determine the interface protocol between the driver and MCU. Refer to the following table for details.
<table>
<tr><td>PS0</td><td>PS1</td><td>Interface</td></tr>
<tr><td>L</td><td>L</td><td>3-wire SPI (write only)</td></tr>
<tr><td>L</td><td>H</td><td>4-wire SPI (write only)</td></tr>
<tr><td>H</td><td>L</td><td>8080 Parallel interface(read and write allowed)</td></tr>
<tr><td>H</td><td>H</td><td>6800 Parallel interface (read and write allowed)</td></tr>
</table>
Note: The above H refers to either VDDIO while L refers VSS</td></tr>
<tr><td>3</td><td>VDD</td><td>This pin is the system power supply pin of the logic block.</td></tr>
<tr><td>4</td><td>PS1</td><td>Like SP0</td></tr>
<tr><td>5</td><td>/CS</td><td>This pin is chip select input.</td></tr>
<tr><td>6</td><td>/RES</td><td>This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>7</td><td>D/C</td><td>This input pin is to identify display data/command cycle.</td></tr>
<tr><td>8</td><td>R/W</td><td>When R/W = “H”: Read.
When R/W = “L”: Write.</td></tr>
<tr><td>9</td><td>E</td><td>This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E)
signal. Read/ write operation is initiated when thispin is pulled high and the chip is selected.
When 8080 interface mode is selected, this pin is the Read (RD) control signal input. Data read operation is
initiated when this pin is pulled low and the chip is selected.</td></tr>
<tr><td>10~17</td><td>DB0~DB7</td><td>8-bit data bus lines</td></tr>
<tr><td>18</td><td>VDD</td><td>This pin is the system power supply pin of the logic block.</td></tr>
<tr><td>19</td><td>VSS</td><td>This is a logic ground pin. It must connect to GND from external supply</td></tr>
<tr><td>20</td><td>VOUT</td><td>This pin is the most positive LCD driving voltage.</td></tr>
<tr><td>21</td><td>C4+</td><td rowspan="8">Connect an external capacitor to these pins when 4X, 5X, 6X or 7X DC-DC Converter Factor is set. Please refer to Figure 13-3 for booster configuration.</td></tr>
<tr><td>22</td><td>C4-</td></tr>
<tr><td>23</td><td>C3+</td></tr>
<tr><td>24</td><td>C3-</td></tr>
<tr><td>25</td><td>C2+</td></tr>
<tr><td>26</td><td>C2-</td></tr>
<tr><td>27</td><td>C1+</td></tr>
<tr><td>28</td><td>C1-</td></tr>
</table>

1.5 Product Outline



PIN	SYMBOL	PIN	SYMBOL
1	VSS	15	DB5
2	PS0	16	DB6
3	VDD	17	DB7
4	PS1	18	VDD
5	/CS	19	VSS
6	/RES	20	VOUT
7	D/C	21	C4+
8	R/W	22	C4−
9	E	23	C3+
10	DB0	24	C3−
11	DB1	25	C2+
12	DB2	26	C2−
13	DB3	27	C1+
14	DB4	28	C1−

1.6 Schematic Diagram



2. Absolute Maximum Ratings

Items	Symbol	MIN.	MAX.	Unit	Condition
Supply Voltage	VDD	-0.3	+3.6	V	Vss = 0V
Input Voltage	VIN	-0.3	VDD+0.3	V	Vss = 0V
Operating Temperature	TOP	0	+50	℃	No Condensation
Storage Temperature	Tst	-10	+60	℃	No Condensation

3. Electrical Characteristics

3.1 DC Characteristics

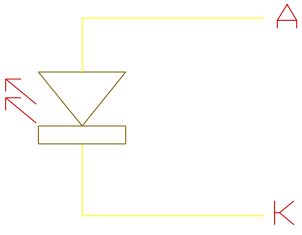
Vss = 0V,Top = 25℃

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Operating Voltage	VDD	3.0	3.3	3.6	V	VDD
Input High Voltage	VIH	0.8 x VDDIO	-	VDDIO	V	/CS1,/RES,A0,E , R/W,D0~D7,C86
Input Low Voltage	VIL	0.0	-	0.1 x VDDIO	V	
Output High Voltage	VOH	0.9 x VDD	-	VDDIO	V	D0~D7
Output Low Voltage	VOL	0.0	-	0.1 x VDDIO	V	D0~D7
Operation Current	Iop	100	-	220	μA	VDD=3.0V
Access mode supply current drain	IAC	-	450	550	μA	Ta=25℃
Display mode supply Current drain	IDP	150	260	450	μA	Ta=25℃

3.2 LED Backlight Circuit

Vss = 0V,Top = 25℃

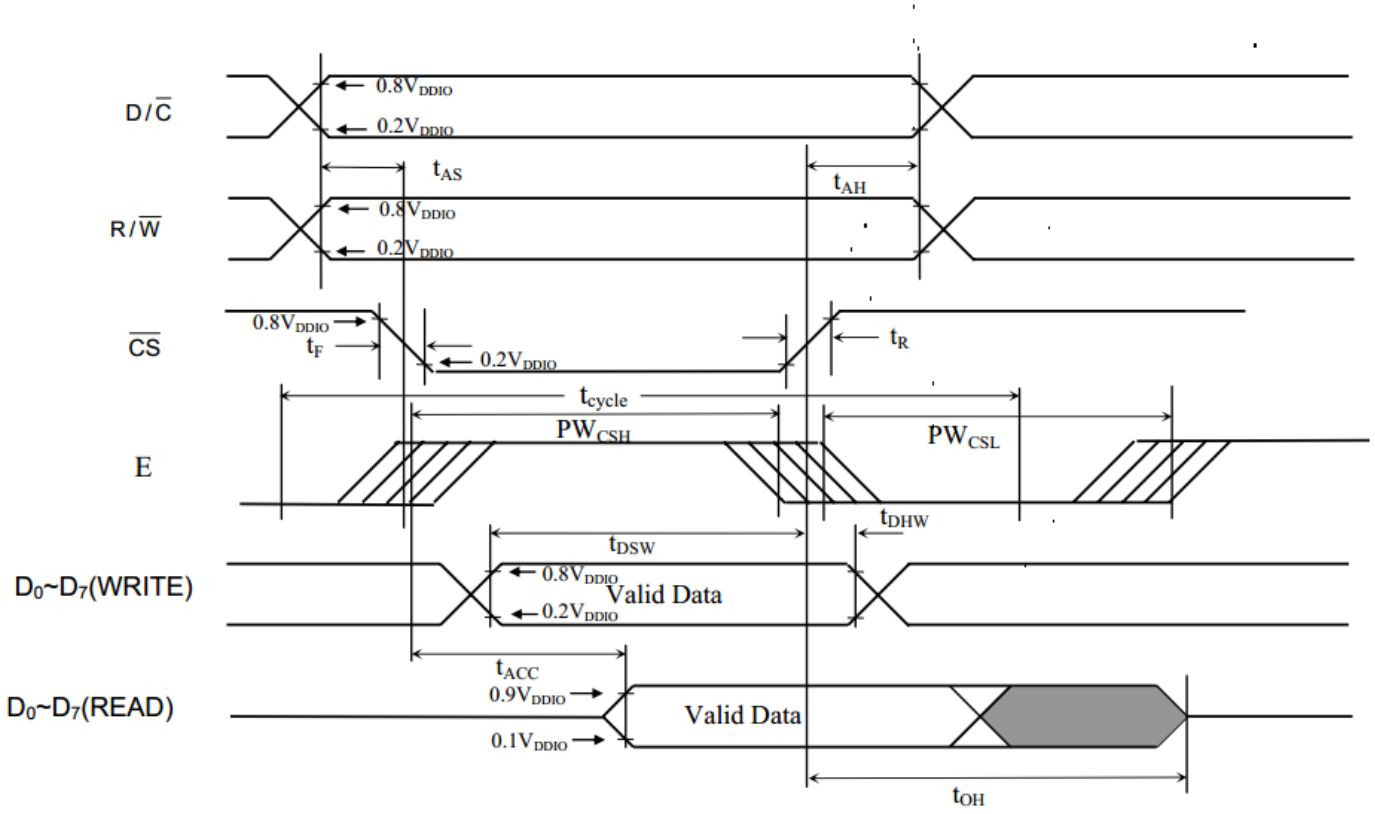
Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Forword Voltage	Vf BLA	-	3.1	-	V	VDD
Forword Current	If BLA	-	10	15	mA	VDD



3.3 AC Characteristics

3.3.1 6800 Mode System Bus Timing

Parallel 6800-series Interface Timing Characteristics (PS0 = H, PS1 = H)



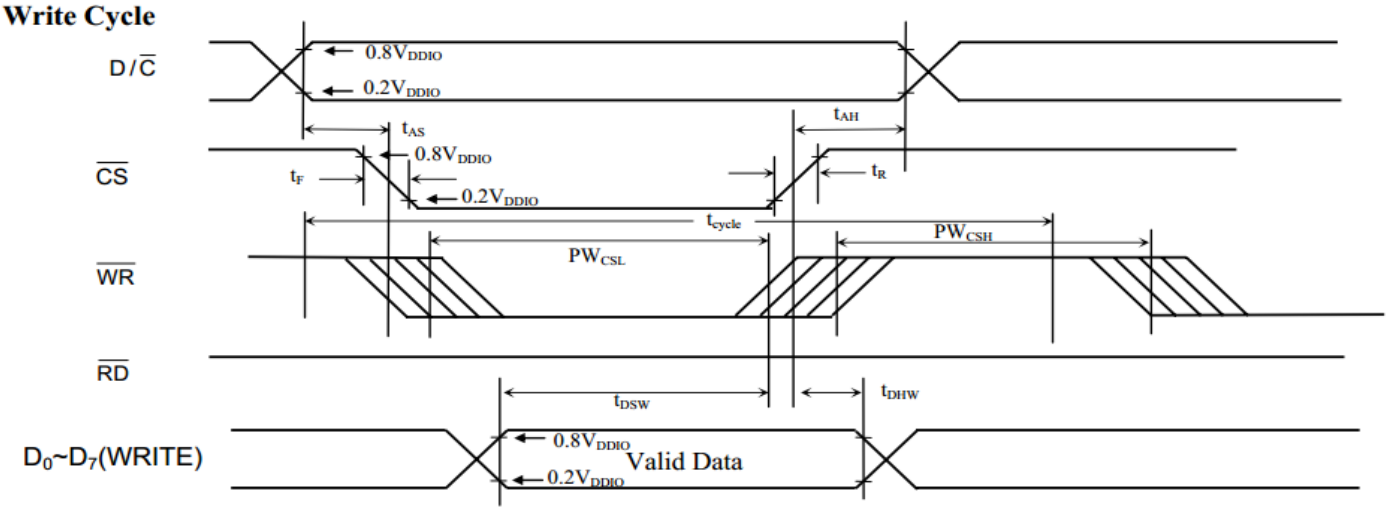
Parallel 6800-series Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	-	100	-	ns
PW_{CSL}	Control Pulse Low Width	-	50	-	ns
PW_{CSH}	Control Pulse High Width	-	50	-	ns
t_F	Fall Time	-	-	10	ns
t_R	Rise Time	-	-	10	ns
t_{AS}	Address Setup Time	-	10	-	ns
t_{AH}	Address Hold Time	-	10	-	ns
t_{DSW}	Data Setup Time	-	60	-	ns
t_{DHW}	Data Hold Time	-	25	-	ns
t_{ACC}	Data Access Time	-	275	-	ns
t_{OH}	Output Hold time	-	125	-	ns

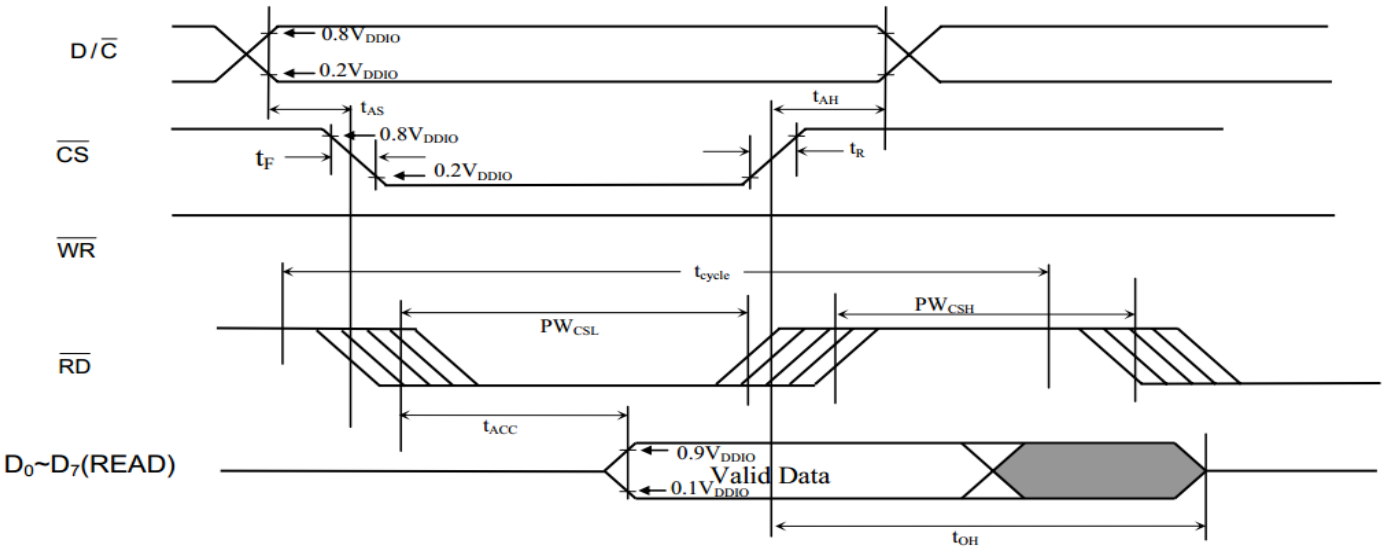
3.3.2 8080ModeSystemBusTiming

Parallel 8080-series Interface Timing Characteristics (PS0 = H, PS1 = L)

Write Cycle

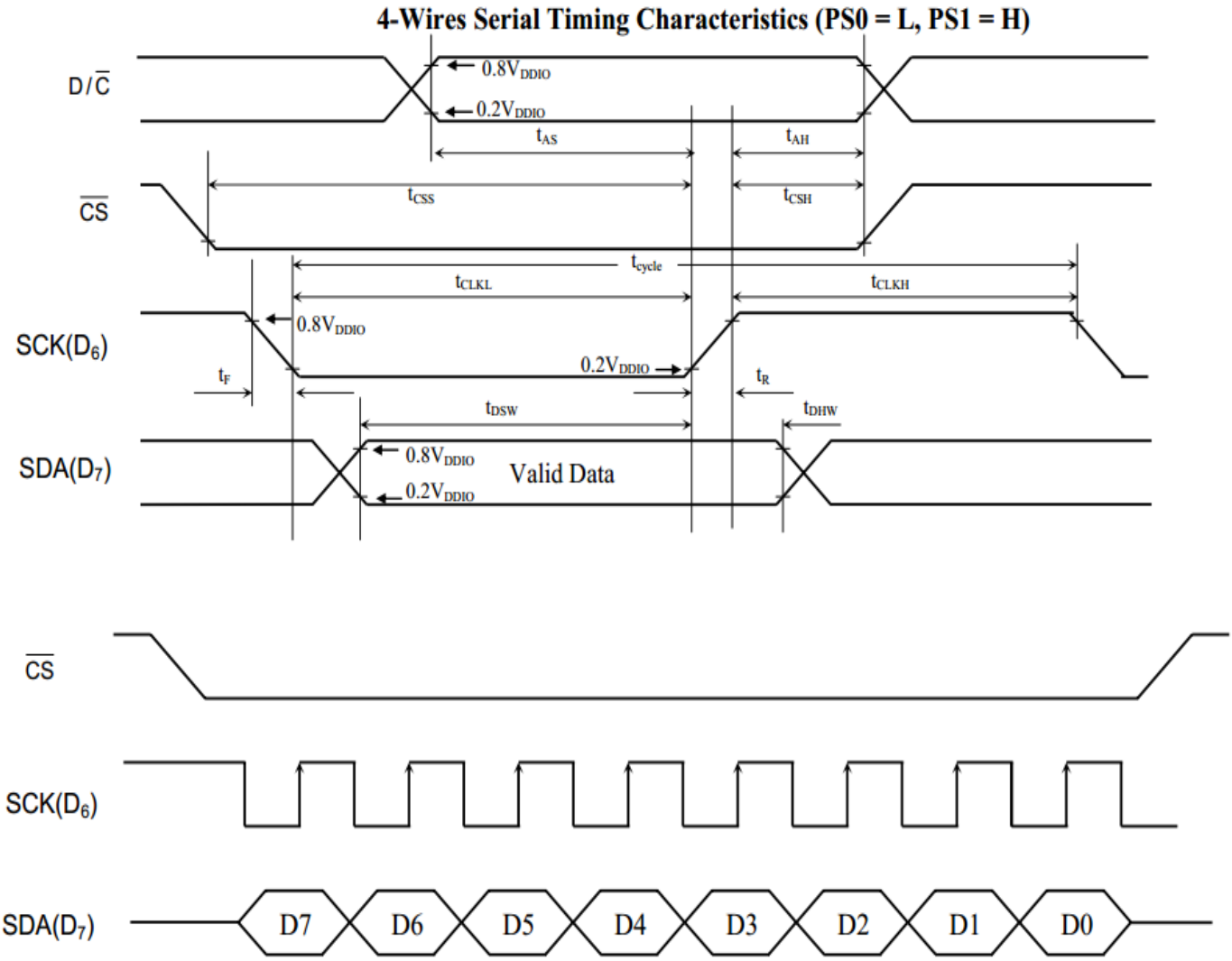


Read Cycle



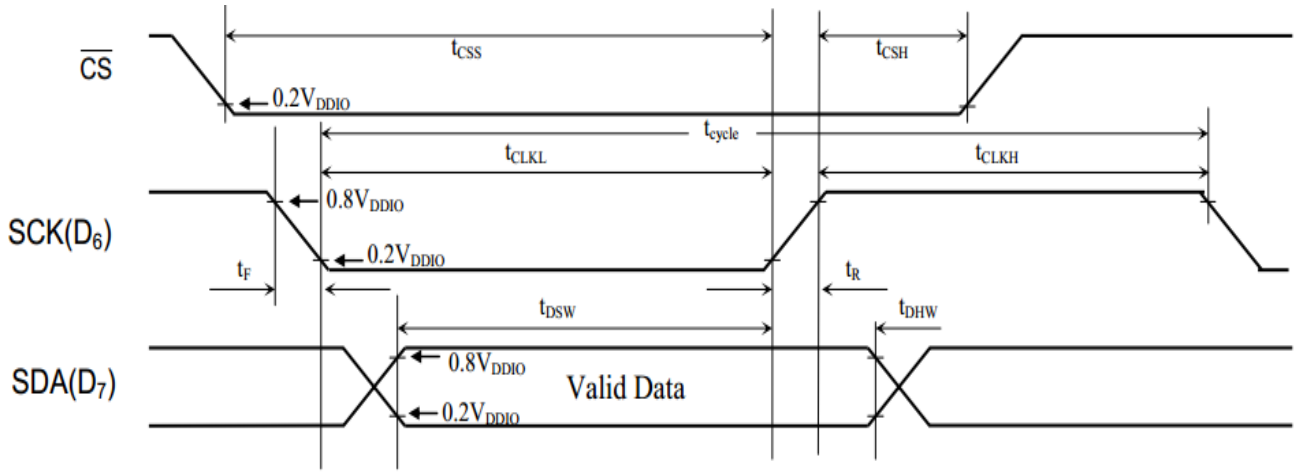
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	-	100	-	ns
PW_{CSL}	Control Pulse Low Width	-	50	-	ns
PW_{CSH}	Control Pulse High Width	-	50	-	ns
t_F	Fall Time	-	-	10	ns
t_R	Rise Time	-	-	10	ns
t_{AS}	Address Setup Time	-	10	-	ns
t_{AH}	Address Hold Time	-	10	-	ns
t_{DSW}	Data Setup Time	-	60	-	ns
t_{DHW}	Data Hold Time	-	25	-	ns
t_{ACC}	Data Access Time	-	275	-	ns
t_{OH}	Output Hold time	-	125	-	ns

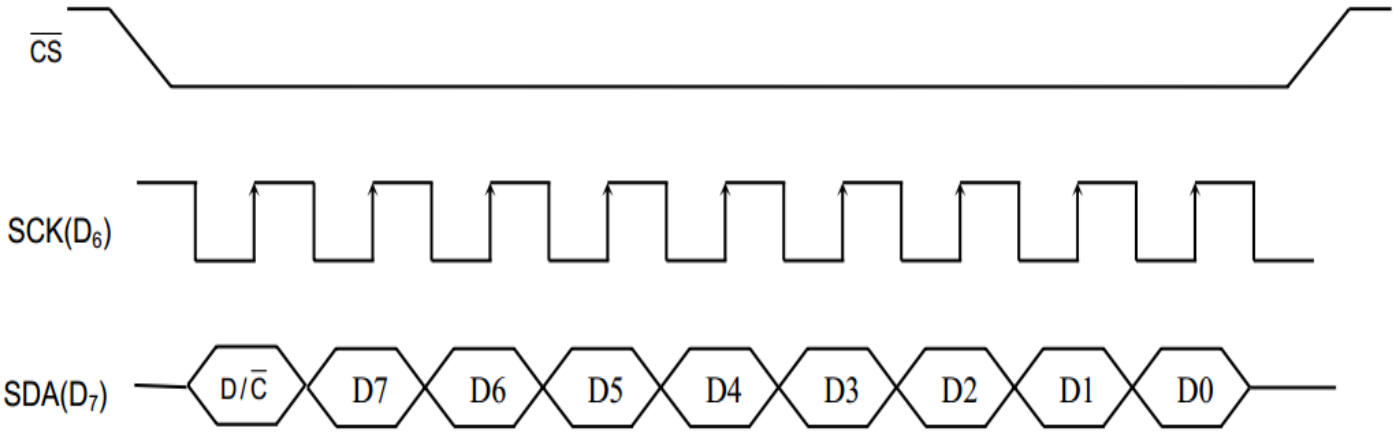
3.3.3 4-Wires Serial Timing Characteristics



Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	-	100	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	10	-	MHz
t_{AS}	Register select Setup Time	20	-	-	ns
t_{AH}	Register select Hold Time	30	-	-	ns
t_{CSS}	Chip Select Setup Time	-	35	-	ns
t_{CSH}	Chip Select Hold Time	-	50	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{DHW}	Write Data Hold Time	10	-	-	ns
t_F	Fall Time	-	-	10	ns
t_R	Rise Time	-	-	10	ns
t_{CLKL}	Clock Low Time	-	50	-	ns
t_{CLKH}	Clock High Time	-	50	-	ns

3.3.4 3-Wires Serial Timing Characteristics





Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	-	100	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	10	-	MHz
t_{CSS}	Chip Select Setup Time	-	35	-	ns
t_{CSH}	Chip Select Hold Time	-	50	-	ns
t_{DSW}	Write Data Setup Time	-	35	-	ns
t_{OHW}	Write Data Hold Time	-	50	-	ns
t_F	Fall Time	-	-	10	ns
t_R	Rise Time	-	-	10	ns
t_{CLKL}	Clock Low Time	-	50	-	ns
t_{CLKH}	Clock High Time	-	50	-	ns

4. Function specifications

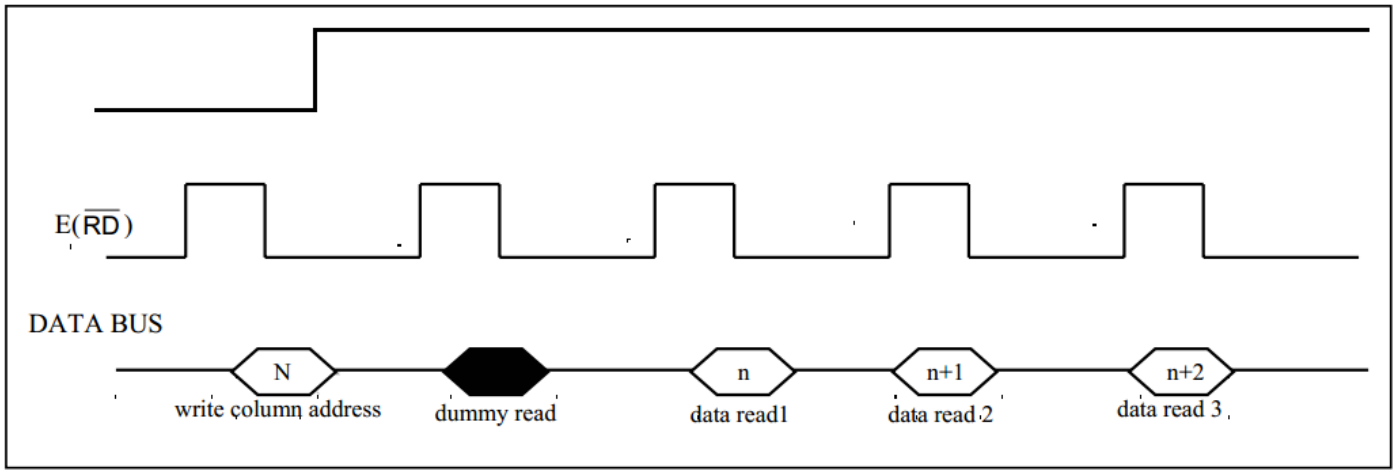
4.1 Microprocessor Interface Logic

The Microprocessor Interface unit consists of three functional blocks for driving the 6800-series parallel interface, 8080-series parallel interface, 3-lines serial peripheral interface and4-lines serial peripheral interface. The selection of different interface is done by PS0 to PS1 pins. Please refer to the pin descriptions on page 14.

MPU Parallel 6800-series Interface
The parallel Interface consists of 8 bi-directional data pins (D7– D0), W / R , C / D , E, CS. W / R (WR) input high indicates a read operation from the Graphical Display Data RAM (GDDRAM) or the status register. W / R input low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of C / D input. The E input serves as data latch signal (clock) when high provided that CS is low. Please refer to Figure 12-1 on page 52 for Parallel Interface Timing Diagram of 6800-series microprocessors.

In order to match the operating frequency of the GDDRAM with that of the MCU, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in the following figure.

Display data



MPU Parallel 8080-series Interface
The parallel interface consists of 8 bi-directional data pins D7 – D0, RD, WR, C / D , CS. RD input serves as data read latch signal (clock) when low provided that CS is low. Whether reading the display data from GDDRAM or reading the status from the status register is controlled by C / D . WR input serves as data write latch signal (clock) when low provided that CS is low. Whether writing the display data to the GDDRAM or writing the command to the command register is controlled by C / D . A dummy read is also required before the first actual display data read for 8080-series interface. Please refer to Figure 12-2 on page 53 for Parallel Interface Timing Diagram of 8080-series microprocessors

MPU 4-wires Serial Peripheral Interface

The 4-wires serial peripheral Interface consists of serial clock SCK, serial data SDA, C / D , CS. SDA is shifted into 8-bit shift register on every rising edge of SCK in the order of data bit 7, data bit 6 …… data bit 0. C / D is sampled on every eighth clock to determine whether the data byte in the shift register is written to the Display Data RAM or command register at the same clock. Please refer to Figure 12-3 on page 54 for 4-wires serial interface timing.

MPU 3-wires Serial Peripheral Interface

The operation is similar to 4-wires serial peripheral interface while C / D is not used. There are AI together 9-bits will be shifted into the shift register on every ninth clock in sequence: C / D bit, D7 to D0 bit. The C / D bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (C / D bit = 1) or the command register (C / D bit = 0). Please refer to Figure 12-4 on page 55 for 3-wires serial interface timing

4.2 Basic Setting

To drive the LCD module correctly and provide normally display, please use the following seting

1> ADC = 0 (normal)
2> SHL select = 1(reverse)
3> LCD Bias Select = 1/9
4> Initial Display Line = 0
5> Entire Display ON/OF = OFF(normal)
6> Reverse Display ON/OF = OFF(normal)
7> Set Power Control Set:
Voltage follower = ON,voltage converter = ON,Voltage regulator = ON
8> Display ON/OF =ON

4.3 Resetting the LCD module

The LCD module should be initialized bu using /RES terminal.
While turning on the VDD and VSS power supply, maintain /RES terminal at LOW level, After the Power supply stabilized, release the reset terminal(/RES = High)

4.4 Display Memory Map

LCD Read Direction	P11 = 0	Column 0				Column 1				.....	Column 23				Column 24			
	Data / Page	D7 D6	D5 D4	D3 D2	D1 D0	D7 D6	D5 D4	D3 D2	D1 D0		D7 D6	D5 D4	D3 D2	D1 D0	D7 D6	D5 D4	D3 D2	D1 D0
BLOCK	P10 = 0																	
0	0								.....									
	1								.....									
	2								.....									
	3								.....									
1	4								.....									
	5								.....									
	6								.....									
	7								.....									
:	:								:									
:	:								:									
:	:								:									
:	:								:									
:	:								:									
:	:								:									
:	:								:									
:	:								:									
:	:								:									
23	88								.....									
	89								.....									
	90								.....									
	91								.....									
24	92								.....									
	93								.....									
	94																	
	95																	

COMMON OUTPUTS

COM17
COM18
COM19
COM20
COM21
:
:
:
:
COM62
COM63
COM64
COM129
COM128
COM127
:
:
:
:
:
COM85
COM84
COM83
COM82

SEGMENT OUTPUTS

SEG129	SEG128	SEG127	SEG126	SEG125	SEG124	SEG123	SEG122	.....	.....	.....	SEG41	SEG40	SEG39	SEG38	SEG37	SEG36	SEG35	SEG34

Mapping depends on the COM output scan direction

4.5 Display Commands

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1 1	15	0 0 0	0 0 0	0 X_5 Y_5	1 X_4 Y_4	0 X_3 Y_3	1 X_2 Y_2	0 X_1 Y_1	1 X_0 Y_0	Set Column Address	Set the start column address by $X_5X_4X_3X_2X_1X_0$ Set the end column address by $Y_5Y_4Y_3Y_2Y_1Y_0$ Column address = 00000000b (POR) Column address is in a range of 0~32 (0x00~0x20).
0 1 1	75	0 X_7 Y_7	1 X_6 Y_6	1 X_5 Y_5	1 X_4 Y_4	0 X_3 Y_3	1 X_2 Y_2	0 X_1 Y_1	1 X_0 Y_0	Set Page Address	Set the start page address by $X_7X_6X_5X_4X_3X_2X_1X_0$ Set the end page address by $Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$ Page address = 00000000b (POR) Page address is in a range of 0~129 (0x00~0x81).
0 1	BB	1 *	0 *	1 *	1 *	1 *	0 X_2	1 X_1	1 X_0	Set COM Output Scan Direction	X_2 X_1 X_0 ROW0…ROW64 ROW65…ROW129 0 0 0 COM0 ->COM64 COM65-> COM129(POR) 0 0 1 COM0->COM64 COM129<-COM65 0 1 0 COM64<-COM0 COM65->COM129 0 1 1 COM64<-COM0 COM129<-COM65

<table>
<tr><th>D/C</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>BC</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Set Data Output Scan Direction and Grayscale</td><td>a) Normal or Reverse page/column/RAM access/scan directions
P_{10} = 0: set page address to normal display (POR)
P_{10} = 1: set page address to inverse display
P_{11} = 0: set column address to normal rotation (POR)
P_{11} = 1: set column address to inverse rotation
P_{12} = 0: set scan direction to column scan(POR)
P_{12} = 1: set scan direction to page scan
P_{13} = 0: set normal scan direction (POR)
P_{13} = 1: set inverse scan direction

b) Gray-scale setting
X = Light gray PWM count (POR 5 counts)
Y = Dark gray PWM count (POR 10 counts)
$P_{22}P_{21}P_{20}$ = X -1 (POR 100)
$P_{25}P_{24}P_{23}$ = Y - X - 1 (POR 100)
Remark: Y-X≤8

* Remarks: The PWM count for White and Black are 0 and 15 respectively.

P_{30} = 0: PWM (POR)

P_{34} = 0:

<table>
<tr><td>White</td><td>Light Gray</td><td>Dark Gray</td><td>Black</td></tr>
<tr><td>0%</td><td>33%</td><td>66%</td><td>100%</td></tr>
</table>

P_{34} = 1:

<table>
<tr><td>White</td><td>Light Gray</td><td>Dark Gray</td><td>Black</td></tr>
<tr><td>0%</td><td>X/15</td><td>Y/15</td><td>100%</td></tr>
</table>

P_{30} = 1: FRC

P_{31} = 0: 3-frame FRC (POR)

<table>
<tr><td>White</td><td>Light Gray</td><td>Dark Gray</td><td>Black</td></tr>
<tr><td>0%</td><td>33%</td><td>66%,</td><td>100%</td></tr>
</table>

P_{31} = 1: 4-frame FRC

<table>
<tr><td>P_{33} P_{32}</td><td>White</td><td>Light Gray</td><td>Dark Gray</td><td>Black</td></tr>
<tr><td>00(POR)</td><td>0%</td><td>25%</td><td>75%,</td><td>100%</td></tr>
<tr><td>01</td><td>0%</td><td>50%</td><td>75%</td><td>100%</td></tr>
<tr><td>10</td><td>0%</td><td>25%</td><td>50%</td><td>100%</td></tr>
<tr><td>11</td><td colspan="4">Reserved</td></tr>
</table>
</td></tr>
<tr><td>1</td><td></td><td>*</td><td>*</td><td>*</td><td>*</td><td>P_{13}</td><td>P_{12}</td><td>P_{11}</td><td>P_{10}</td><td></td><td></td></tr>
<tr><td>1</td><td></td><td>*</td><td>*</td><td>P_{25}</td><td>P_{24}</td><td>P_{23}</td><td>P_{22}</td><td>P_{21}</td><td>P_{20}</td><td></td><td></td></tr>
<tr><td>1</td><td></td><td>*</td><td>*</td><td>*</td><td>P_{34}</td><td>P_{33}</td><td>P_{32}</td><td>P_{31}</td><td>P_{30}</td><td></td><td></td></tr>
</table>

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1 1 1	CA	1 0 * 0	1 0 * 0	0 0 Y_5 0	0 0 Y_4 0	1 0 Y_3 0	0 0 Y_2 0	1 0 Y_1 0	0 0 Y_0 0	Set Display Control	Driver duty selection Select driver duty from 1/16 to 1/128. As $Y_5Y_4Y_3Y_2Y_1Y_0$ is increased from 000011b to 011111b, the number of display lines, N is increased at the same rating. To specify the $Y_5Y_4Y_3Y_2Y_1Y_0$ = (N/4)-1 where 1/N is the driver duty. $Y_5Y_4Y_3Y_2Y_1Y_0$= 100000b for 1/130 duty.
0 1 1 1 1	AA	1 X_7 Y_7 Z_7 *	0 X_6 Y_6 Z_6 *	1 X_5 Y_5 Z_5 *	0 X_4 Y_4 Z_4 *	1 X_3 Y_3 Z_3 *	0 X_2 Y_2 Z_2 *	1 X_1 Y_1 Z_1 P_{41}	0 X_0 Y_0 Z_0 P_{40}	Set Area Scroll	a) Top Block Address $X_7X_6X_5X_4X_3X_2X_1X_0$ is used to specify the row address at the top of the scrolling area. Top row address = 00000000b (POR) b) Bottom Block Address $Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$ is used to specify the row address at the bottom of the scrolling area. Bottom row address = 00000000b (POR) c) Number of specified Blocks The number of specified blocks = Number of (Top fixed area + Scroll area) blocks –1. If bottom scroll or whole screen scroll mode is chosen, the number of specified blocks is set to $Z_7Z_6Z_5Z_4Z_3Z_2Z_1Z_0$ Number of specified blocks = 00000000b (POR) d) Area Scroll Mode There are four types of area scroll. P_{41} P_{40} Types of Area Scroll 0 0 Center Screen Scroll 0 1 Top Screen Scroll 1 0 Bottom Screen Scroll 1 1 Whole Screen Scroll Type of area scroll = Whole Screen Scroll (POR)
0 1	AB	1 X_7	0 X_6	1 X_5	0 X_4	1 X_3	0 X_2	1 X_1	1 X_0	Set Scroll Start	$X_5X_4X_3X_2X_1X_0$ specify the start row address of area scrolling. Start block address = 00000000b (POR)
0 1	20	0 *	0 *	1 *	0 X_4	0 X_3	0 X_2	0 X_1	0 X_0	Set Power Control Register	X_0=0: turns off the reference voltage generator (POR) X_0=1: turns on the reference voltage generator X_1=0: turns off the internal regulator and voltage follower (POR) X_1=1: turns on the internal regulator and voltage follower Select booster level X_4 X_3 X_2 Boost level 0 0 0 4X 0 0 1 5X 0 1 0 6X (POR) 0 1 1 7X

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1 1	81	1 * *	0 * *	0 X_5 *	0 X_4 *	0 X_3 *	0 X_2 Y_2	0 X_1 Y_1	1 X_0 Y_0	Set Contrast Level & Internal Regulator Resistor Ratio	a) Select contrast level from 64 contrast steps Contrast increases as $X_5X_4X_3X_2X_1X_0$ is increased from 000000b to 111111b. $X_5X_4X_3X_2X_1X_0$ = 100000b (POR) b) The internal regulator gain (1+R2/R1) V_{OUT} increases as $Y_2Y_1Y_0$ is increased from 000b to 111b. The factor, 1+R2/R1, is given by: $Y_2Y_1Y_0$ = 000: 3.38 (POR) $Y_2Y_1Y_0$ = 001: 4.41 $Y_2Y_1Y_0$ = 010: 5.44 $Y_2Y_1Y_0$ = 011: 6.47 $Y_2Y_1Y_0$ = 100: 7.50 $Y_2Y_1Y_0$ = 101: 8.52 $Y_2Y_1Y_0$ = 110: 9.55 $Y_2Y_1Y_0$ = 111: 10.58
0 1 1	A8	1 0 X_7	0 0 X_6	1 0 X_5	0 0 X_4	1 0 X_3	0 0 X_2	0 0 X_1	0 0 X_0	Enter partial Display	$X_7X_6X_5X_4X_3X_2X_1X_0$: End COM Address = 00000000b (POR)
0	A9	1	0	1	0	1	0	0	1	Exit partial Display	Exit the "partial display mode" by executing the command 10101001b (POR)
0	AE - AF	1	0	1	0	1	1	1	X_0	Set Display On/Off	X_0=0: turns off LCD panel (POR) X_0=1: turns on LCD panel
0	94 - 95	1	0	0	1	0	1	0	X0	Enter/Exit sleep mode	X0=0: exit the sleep mode. X0=1: enter sleep mode. (POR)
0	D1 – D2	1	1	0	1	0	0	X_1	X_0	Enable/disable internal oscillator	X_1 X_0 Internal oscillator status 0 1 ON 1 0 OFF (POR)
0 1	82	1 *	0 *	0 *	0 *	0 *	0 *	1 X_1	0 X_0	Set temperature compensation coefficient	VOUT average temperature gradients X_1 X_0 Average Temperature Gradient [%/oC] 0 0 -0.01 (POR) 0 1 -0.06
0	25	0	0	1	0	0	1	0	1	NOP	Command result in No Operation The command should be issued after the execution of the Status Read command
0 1	5C	0 Y_{71}	1 Y_{61}	0 Y_{51}	1 Y_{41}	1 Y_{31}	1 Y_{21}	0 Y_{11}	0 Y_{01}	Write display data	Enter the "write display data mode" by executing the command 01011100b. The following byte is used to specify the data byte to be written to the GDDRAM directly. The D/C bit should be stated at logic "1" during the display data is written to the GDDRAM.

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0/1	FB	1 L_0	1 0	1 0	1 0	1 B_3	0 B_2	1 B_1	1 B_0	Set biasing ratio & Command lock/unlock	Allow user to set bias from 1/ 4 to 1/13 $B_3B_2B_1B_0$ Bias ratio 1 0 0 1 1/4 bias 1 0 0 0 1/5 bias 0 1 1 1 1/6 bias 0 1 1 0 1/7 bias 0 1 0 1 1/8 bias 0 1 0 0 1/9 bias 0 0 1 1 1/10 bias 0 0 1 0 1/11 bias 0 0 0 1 1/12 bias 0 0 0 0 1/13 bias (POR) L_0 Lock and unlock Cmd 0 unlock (POR) 1 lock and no more cmd/data is written to driver The 2nd byte is sent as Cmd if L_0 is set to 1
0 1 1	F2	1 0 X_0	1 1 N_6	1 F_4 N_5	1 F_3 N_4	0 F_2 N_3	0 F_1 N_2	1 F_0 N_1	0 0 N_0	Set Frame frequency and N-line Inversion	This command uses to change the frame frequency; set the N-line inversion and N-line inversion mode X_0 = 1 (POR) X_0 = 0 $F_4F_3F_2F_1F_0$ 00000 : 56.4 Hz (POR) 64Hz 00111 : +10.1% +11.8% 01000 : +10.7% +15.2% 01001 : +12.5% +15.2% 01010 : +14.1% +20.6% 01011 : +16.1% +20.6% 01100 : +17.4% +25.9% 01101 : +19.5% +25.9% 01110 : +21.4% +32.9% 01111 : +23.7% +32.9% 10000 : +24.6% +37.4% 10001 : +27.1% +37.4% 10010 : +29.2% +46.0% 10011 : +31.8% +46.0% 10100 : +33.6% +54.6% 10101 : +36.5% +54.6% 10110 : +39.0% +66.9% 10111 : +42.2% +66.9% 11000 : +43.2% +75.8% 11001 : +46.6% +75.8% 11010 : +49.7% +94.0% Remark: The frame frequency is typical value for 130mux and PWM mode. The second byte data $N_5N_4N_3N_2N_1N_0$ sets the n-line inversion register from 2 to 64 lines to reduce display crosstalk. Register values from 000001b to 111111b are mapped to 2 lines to 64 lines respectively. Value 00000b disables the N-line inversion. 010000 is the POR value. To avoid a fix polarity at some lines, it should be noted that the total number of mux should NOT be a multiple of the lines of inversion (n). N_6 0 – reset n-line counter per frame (POR) 1 – will not reset n-line counter per frame

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1 1	F6	1 Y_2 0	1 Y_1 0	1 0 0	1 X_4 0	0 X_3 0	1 X_2 1	1 X_1 1	0 X_0 0	Dual OTP setting	This command set the offset value of contrast for the first time and the second time OTP $X_4X_3X_2X_1X_0$ (Emulate/Program) 00000 : original contrast (+ 0 fine step/ -1 fine step) 00001 : original contrast (+ 1 fine step/ -2 fine steps) 00010 : original contrast (+ 2 fine steps/ -3 fine steps) 00011 : original contrast (+ 3 fine steps/ -4 fine steps) 00100 : original contrast (+ 4 fine steps/ -5 fine steps) 00101 : original contrast (+ 5 fine steps/ -6 fine steps) 00110 : original contrast (+ 6 fine steps/ -7 fine steps) 00111 : original contrast (+ 7 fine steps/ -8 fine steps) 01000 : original contrast (+ 8 fine steps/ -9 fine steps) 01001 : original contrast (+ 9 fine steps/ -10 fine steps) 01010 : original contrast (+10 fine steps/-11 fine steps) 01011 : original contrast (+11 fine steps/-12 fine steps) 01100 : original contrast (+12 fine steps/-13 fine steps) 01101 : original contrast (+13 fine steps/-14 fine steps) 01110 : original contrast (+14 fine steps/-15 fine steps) 01111 : original contrast (+15 fine steps/-16 fine steps) 10000 : original contrast (–16 fine steps/+15 fine steps) 10001 : original contrast (- 15 fine steps/+14 fine steps) 10010 : original contrast (- 14 fine steps/+13 fine steps) 10011 : original contrast (- 13 fine steps/+12 fine steps) 10100 : original contrast (- 12 fine steps/+11 fine steps) 10101 : original contrast (- 11 fine steps/+10 fine steps) 10110 : original contrast (- 10 fine steps/+ 9 fine steps) 10111 : original contrast (- 9 fine steps/+ 8 fine steps) 11000 : original contrast (- 8 fine steps/+ 7 fine steps) 11001 : original contrast (- 7 fine steps/+ 6 fine steps) 11010 : original contrast (- 6 fine steps/+ 5 fine steps) 11011 : original contrast (- 5 fine steps/+ 4 fine steps) 11100 : original contrast (- 4 fine steps/+ 3 fine steps) 11101 : original contrast (- 3 fine steps/+ 2 fine steps) 11110 : original contrast (- 2 fine steps/+ 1 fine step) 11111 : original contrast (- 1 fine step/+ 0 fine step) $Y_1 = 0$: 1st Level OTP (POR) $Y_1 = 1$: 2nd Level OTP $Y_2 = 0$: Emulate OTP step $Y_2 = 1$: Enable OTP (POR) Remarks: 2nd level OTP cannot be executed before 1st level OTP. $Y_2Y_1 = 00$, $X_3X_2X_1X_0 = 0000$: Disable OTP function * Note: 1 contrast step = 2 fine steps
0	F8	1	1	1	1	1	0	0	0	OTP programming	This command starts to program LCD driver with OTP offset value. This command can be executed twice only. Detail of OTP programming procedure on page 36
0 1	44	0 A_7	1 A_6	0 A_5	0 A_4	0 A_3	1 A_2	0 A_1	0 A_0	Set 1st Com Line	Set 1st Com-line command. Byte A specifies the number of scroll lines. $A_7A_6A_5A_4A_3A_2A_1A_0$ = 00000000 (POR) Byte A is ranging from 0 to 129

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	F7	1	1	1	1	0	1	1	1	Grayscale or mono mode selection	$Y_0 = 0$: Grayscale mode (POR) $Y_0 = 1$: Mono mode
1		0	0	0	0	0	0	0	0		
1		0	0	0	0	1	1	1	0		
1		0	Y_0	0	0	0	0	0	1		

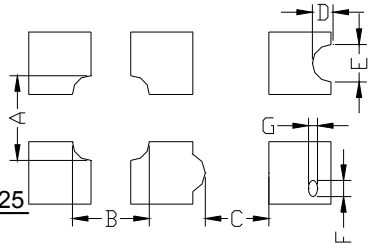
D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	5D	0	1	0	1	1	1	0	1	Read display data	Enter the "read display data mode" by executing the command 01011101b. The next byte is a dummy data. The GDDRAM data will be read form the second byte. The GDDRAM column address pointer will be increased by one automatically after each 2-bytes data read.
1		Y_{71}	Y_{61}	Y_{51}	Y_{41}	Y_{31}	Y_{21}	Y_{11}	Y_{01}		
0	F3	1	1	1	1	0	0	1	1	Bias current, booster frequency & OTP status read selection	This command selects the bias current for VL5, VL4, VL3 and VL2, the booster frequency and the 1st and 2nd OTP status read. A_2 A_1 A_0: bias current for VL3 and VL2 A_6 A_5 A_4: bias current for VL5 and VL4 000 : 1.0 x I_{ref} 001 : 3.5 x I_{ref} 010 : 6.0 x I_{ref} (POR) 011 : 8.5 x I_{ref} 100 : 11.0 x I_{ref} 101 : 13.5 x I_{ref} 110 : 17.0 x I_{ref} 111 : 18.5 x I_{ref} X_1X_0 00 : Fosc/2 (POR) 01 : Fosc/4 10 : Fosc/8 11 : Fosc/16 $Y_2Y_1Y_0 = 000$: Read 1st Level OTP (POR) $Y_2Y_1Y_0 = 111$: Read 2nd Level OTP where I_{ref} is a constant
1		1	A_6	A_5	A_4	0	A_2	A_1	A_0		
1	15	0	0	0	1	0	1	0	1		
1	00	0	0	0	0	0	0	0	0		
1		1	0	0	Y_2	Y_1	Y_0	X_1	X_0		
0	F9	1	1	1	1	1	0	0	1	Read back dual OTP value, SSL module identity & OTP register status	A_4 A_3 A_2 A_1 A_0 = OTP value
0		*	*	*	A_4	A_3	A_2	A_1	A_0		

4.6 Basic Operating Sequence

```
void intial(void)

{
     Comwrite(0xd1);    //Internal oscillator ON
    Comwrite(0x94);    //exit the sleep mode
     delay(10);
    Comwrite(0xf2);
    Datwrite(0x00);
    Datwrite(0x00);

    Comwrite(0xf7);
    Datwrite(0x00);
    Datwrite(0x0e);
    Datwrite(0x01);

    Comwrite(0xBC);
    Datwrite(0x02);
    Datwrite(0x00);
    Datwrite(0x00);

    Comwrite(0x15);    //Set Column    0~32
    Datwrite(0);    //start column address
    Datwrite(24);    //end column address

    Comwrite(0x75);    //Set Page 0~129
    Datwrite(0x00);    //start page address
    Datwrite(0x5F);    //end page address

    Comwrite(0x44);    //Set 1st Com Line
    Datwrite(0x11);

    Comwrite(0xBB);
    Datwrite(0x01);

    Comwrite(0xCA); //Driver duty selection
    Datwrite(0x00);
    Datwrite(0x17);
    Datwrite(0x00);
```

```
    Comwrite(0x20);    //Set Power Control Register
    Datwrite(0x07);
     delay(150);

    Comwrite(0x81);    //Set Contrast Level & Internal Regulator Resistor Ratio
    Datwrite(0x2C);    //X5--X0
    Datwrite(0x05);    //Y2--Y0

    Comwrite(0x82);
    Datwrite(0x01);

    Comwrite(0xFB);    //set bias
    Datwrite(0x02);    //1/11 bias

    Comwrite(0xF3);    //Bias current,
    Datwrite(0xA2);
    Datwrite(0x15);
    Datwrite(0x00);
    Datwrite(0x81);

    Comwrite(0xF2);    //SET Frame frequency
    Datwrite(0x40);
    Datwrite(0x04);
    //Datwrite(0x10);
    //Datwrite(0x01);

    Comwrite(0xAF); //display on

}
```

5. Inspection Standards

Item	Criterion for defects	Defect type
1) Display on inspection	(1) Non display (2) Vertical line is deficient (3) Horizontal line is deficient (4) Cross line is deficient	Major
2) Black / White spot	Size Φ(mm) Acceptable number Φ≤0.3 Ignore (note) 0.3<Φ≤0.45 3 0.45<Φ≤0.6 1 0.6<Φ 0	Minor
3) Black / White line	Length (mm) Width (mm) Acceptable number L≤10 W≤0.03 Ignore 5.0≤L≤10 0.03<W≤0.04 3 5.0≤L≤10 0.04<W≤0.05 2 1.0≤L≤10 0.05<W≤0.06 2 1.0≤L≤10 0.06<W≤0.08 1 L≤10 0.08<W follows 2) point defect Defects separate with each other at an interval of more than 20mm	Minor
4) Display pattern	 $\frac{A+B}{2} \leq 0.28$ | 0<C | $\frac{D+E}{2} \leq 0.25$ | $\frac{F+G}{2} \leq 0.25$ Note: 1) Up to 3 damages acceptable 2) Not allowed if there are two or more pinholes every three-fourth inch.	Minor
5) Spot-like contrast irregularity	Size Φ(mm) Acceptable Number Φ≤0.7 Ignore (note) 0.7<Φ≤1.0 3 1.0<Φ≤1.5 1 1.5<Φ 0 Note: 1) Conformed to limit samples. 2) Intervals of defects are more than 30mm.	Minor
6) Bubbles in polarizer	Size Φ(mm) Acceptable Number Φ≤0.4 Ignore (note) 0.4<Φ≤0.65 2 0.65<Φ≤1.2 1 1.2<Φ 0	Minor
7) Scratches and dent on the polarizer	Scratches and dent on the polarizer shall be in the accordance with "2) Black/white spot", and "3) Black/White line".	Minor
8) Stains on the surface of LCD panel	Stains which cannot be removed even when wiped lightly with a soft cloth or similar cleaning.	Minor
9) Rainbow color	No rainbow color is allowed in the optimum contrast on state within the active area.	Minor
10) Viewing area encroachment	Polarizer edge or line is visible in the opening viewing area due to polarizer shortness or sealing line.	Minor
11) Bezel appearance	Rust and deep damages that are visible in the bezel are rejected.	Minor
12) Defect of land surface contact	Evident crevices that are visible are rejected.	Minor
13) Parts mounting	(1) Failure to mount parts (2) Parts not in the specifications are mounted (3) For example: Polarity is reversed, HSC or TCP falls off.	Minor
14) Part alignment	(1) LSI, IC lead width is more than 50% beyond pad outline. (2) More than 50% of LSI, IC leads is off the pad outline.	Minor
15) Conductive foreign matter (solder ball, solder hips)	(1) 0.45<Φ, N≥1 (2) 0.3<Φ≤0.45, N≥1, Φ: Average diameter of solder ball (unit: mm) (3) 0.5<L, N≥1, L: Average length of solder chip (unit: mm)	Minor
16) Bezel flaw	Bezel claw missing or not bent	Minor

17) Indication on name plate (sampling indication label)	(1) Failure to stamp or label error, or not legible.(all acceptable if legible) (2) The separation is more than 1/3 for indication discoloration, in which the characters can be checked.	Minor

6. Handling Precautions

6.1 Mounting method

A panel of LCD module made by our company consists of two thin glass plates with polarizers that easily get damaged.

And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board (PCB), extreme care should be used when handling the LCD modules.

6.2 Cautions of LCD handling and cleaning

When cleaning the display surface, use soft cloth with solvent (recommended below) and wipe lightly.

-Isopropyl alcohol

-Ethyl alcohol

-Trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

-Water

-Ketene

-Aromatics

6.3 Caution against static charge

The LCD module use C-MOS LSI drivers. So we recommend you:

Connect any unused input terminal to V_{dd} or V_{ss}. Do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

6.4 Packaging

-Module employs LCD elements, and must be treated as such. Avoid intense shock and falls from a height.

-To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

6.5 Caution for operation

-It is an indispensable condition to drive LCD module within the limits of the specified voltage since the higher voltage over the limits may cause the shorter life of LCD module.

-An electrochemical reaction due to DC (direct current) causes LCD undesirable deterioration so that the uses of DC (direct current) drive should be avoided.

-Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD module may show dark color in them. However those phenomena do not mean malfunction or out of order of LCD module, which will come back in the specified operating temperature.

6.6 Storage

In the case of storing for a long period of time, the following ways are recommended:

-Storage in polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with not desiccant.

-Placing in a dark place where neither exposure to direct sunlight nor light is. Keeping the storage temperature range.

-Storing with no touch on polarizer surface by any thing else.

6.7 Safety

-It is recommendable to crash damaged or unnecessary LCD into pieces and to wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.

-When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well at once with soap and water.

7. Packaging Specifications

鑫洪泰 HOT DISPLAY

Packaging Specifications
HTG9696A

Approved	Checked	Designed

7.1 Packaging Material

No	Item	Dimensions(mm)	1PCS Weight(KG)	Quantity	Total Weight	
1	COG	29.9*35.9*2.9	0.015	400	6.0	
2	PE Bag	60*60	0.001	400	0.4	
3	Foam Rubber Cushion	310*170	0.0175	8	0.14	
4	Partition A1	310*170*100	0.30	4	1.2	
5	Product Box	330*180*120(neutral packing)	0.45	4	1.8	
6	Carton	480*390*330(neutral packing)	0.9	1	0.9	
7	Tape			AR		
8	Label Specifications			1		
9	Label Rohs			1		
10	Label ESD			1		

7.2. Total LCD Weight in carton: 10.5 KG±10%

7.3. Packaging Specifications and Quantity:

(1)Quantity Of Spacer:A1*4

(2)Total LCM quantity in carton: quantity per box 100* no of boxes 4 = 400